Co-simulation Verilog – ngspice, example SAR ADC

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Files

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11.01.2024

user provided	adc.cir	ngspice netlist: analog part, digital support, interface with code model, simulation control
	adc.v	digital ADC part, Verilog code
within ngspice distribution	verilator_main.c	main required by Verilator
	verilator_shim.c	structure of shared lib to be linked to d_cosim code model
	vnlnggen	ngspice control language script for creating shared lib adc.so
	digital.cm -> d_cosim	code model, loading adc.so, interface to digital part of netlist
external install; Linux, Windows	Verilator	Verilator (Linux, Windows)
	ngspice	simulator, version 42 and up

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Procedure → two commands only!

Command **ngspice vlnggen adc.v**

- calls Verilator to compile adc.v into adc.c
- calls g++ (msvc) to compile adc.c, verilator_main.c, verilator_shim.c and some other files generated or provided by Verilator, and links them into shared library adc.so (adc.dll)

Command **ngspice adc.cir**

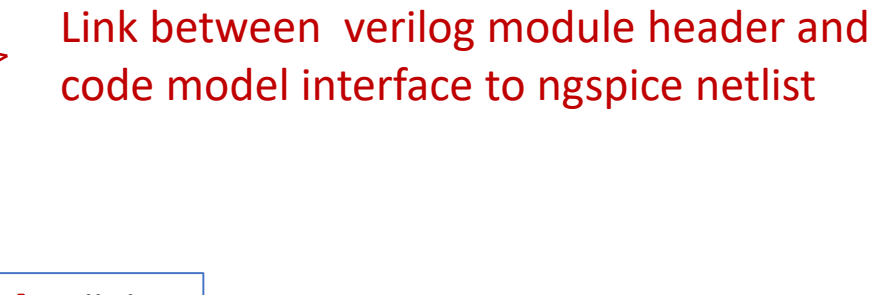
- Load code model d_cosim
- Load netlist adc.cir
  - Load shared lib adc.so
- Run simulation (e.g. transient)
- Save and/or plot data

Verilog

```
module adc(Clk, Comp, Start, Sample, Done, Result);
   input wire Clk, Comp, Start;
   output reg  Sample, Done;
   output reg [Bits - 1 : 0] Result;
   parameter Bits=6;
…
```

Code model

```
adut [ Clk Comp Start] [Sample Valid ~d5 ~d4 ~d3 ~d2 ~d1 ~d0] null dut
.model dut d_cosim simulation="./adc.so"
```



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Links, manual

Example	https://sourceforge.net/p/ngspice/ngspice/ci/master/tree/examples/xspice/verilator/
Sources	https://sourceforge.net/p/ngspice/ngspice/ci/master/tree/src/xspice/verilog/
Help	https://sourceforge.net/p/ngspice/discussion/127605/
Manual	https://ngspice.sourceforge.io/docs/ngspice-42-manual.pdf Chapters • 12.4.25 d_cosim • 14.3 Digital devices defined by a Hardware Description Language